V-Band High-Power Low Phase-Noise Monolithic Oscillators and Investigation of Low Phase-Noise Performance at High Drain Bias

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***Abstract*— This paper reports on the excellent performance of V-band monolithic high electron-mobility transistor (HEMT) oscillators, and discusses oscillation characteristics on drain bias. With regard to output characteristics, double-hetero (DH) HEMT (especially with a high-density Si-planar doped layer) are superior to single-hetero (SH) HEMT's. A monolithic microwave integrated circuit (MMIC) oscillator has been developed with a planar doped DH HEMT and has achieved the peak output power of 11.1 dBm at a 55.9-GHz oscillation frequency. Phase noise of −85 dBc/Hz at 100-kHz offset and −103 dBc/Hz at 1-MHz offset have been achieved at a drain voltage of 5.5 V and a gate voltage of 0 V. These characteristics have been achieved without any buffer amplifiers or dielectric resonators. This study has revealed that the phase noise decreases as drain voltage increases. This phenomenon is caused by lower pushing figure and lower noise level at a low-frequency range obtained under a high drain voltage. It is because the depletion layer in the channel is extended to the drain electrode with increase of drain voltage, resulting in the small fluctuation of the gate-to-source capacitance. We also investigate low-frequency noise spectra of AlGaAs/InGaAs/GaAs DH HEMT's with different bias conditions. The low-frequency noise decreases for more than 3 V of the drain voltage. A unique mechanism is proposed to explain this phase noise reduction at high drain voltage.**

***Index Terms*—Drain bias, HEMT, MMIC's, phase noise.**

I. Introduction

OSCILLATORS are key components for microwave and millimeter-wave communication systems requiring low phase-noise characteristics as well as high output power. Recently, demand for millimeter-wave communication systems is increasing, along with development of millimeter-wave local area networks (LAN's), collision-avoidance radar, etc. [1]–[3]. Fundamental oscillators are preferred for such systems because they are of a small-size and are less costly. Metal–semiconductor field-effect transistors (MESFET's), High electron-mobility transistors (HEMT's), and heterojunction bipolar transistors (HBT's) are widely used as active devices for microwave and millimeter-wave applications. However, the low-frequency noise is relatively high in field-effect transistors (FET's) and HEMT's, which have been used in conventional oscillators. From the viewpoint of the low-frequency noise, HBT's are preferable devices for oscillators because they are bulk-type devices and are less affected by the surface conditions. However, HEMT's have superior high-frequency performance compared to HBT's which indicates that monolithic HEMT oscillators are more suited for multifunction applications when integrated on a single chip. In addition, Zhang *et al.* reported that the phase noise of HEMT oscillators is superior to that of HBT oscillators because the up-conversion factor of HBT oscillators is much larger than that of HEMT oscillators, even though the low-frequency noise of HBT's is substantially lower [4].

Many ways to improve oscillator phase noise have been proposed. There have been several successful developments using dielectric resonators assembled on monolithic microwave integrated circuits (MMIC's) or off-chip [5], [6]. The problem in these oscillators is the difficulty in placing a dielectric resonator in plane. Phase-locked oscillators (PLO's) have good phase-noise performances near carrier frequencies. However, PLO's need several integrated circuits (IC's) like divider IC's, thus, these oscillators become big and manufacturing costs are relatively high. Fundamental monolithic oscillators are preferred for one of solutions to smaller size and lower cost.

Meanwhile, the mechanisms that generate the phase noise of the oscillators have been investigated by many researchers. Major factors that decide phase-noise performance are a pushing figure and an up-conversion factor [4], [7]–[13]. There have been many papers published regarding up-conversion of the low-frequency noise due to nonlinearity. Verdier *et al.* investigated dependence of the up-conversion factors on gate–source voltage [7]. Although these researchers suggest very important points, there are few reports among them on the dependence of the phase noise on drain biases.

In this paper, a comparison of the oscillation performance of several GaAs pseudomorphic high electron-mobility transistor (pHEMT) based oscillators are performed at V-band. As a result, excellent performances are obtained in the oscillators using AlGaAs/InGaAs double-hetero (DH) pHEMT's. Measured phase-noise performance is comparable with InP HBT-based monolithic oscillators. A phenomena in which phase noise improves at a high drain voltage is also described.

Manuscript received October 29, 1997; revised February 23, 1998.

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Publisher Item Identifier S 0018-9480(98)06729-5.

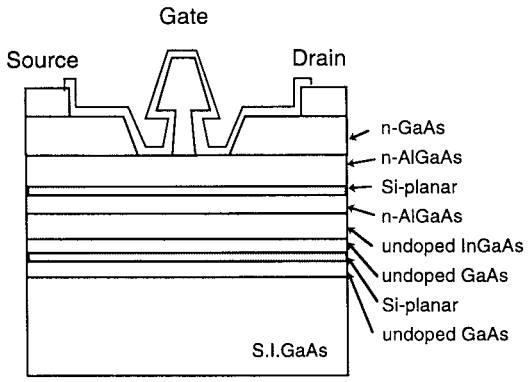


Fig. 1. Cross-sectional view of an AlGaAs/InGaAs DH HEMT. the SH HEMT has no GaAs layer under the InGaAs and Si-planar doped layer in the GaAs layer.

TABLE I
CARRIER DENSITY OF SI-PLANAR DOPED LAYER

Device	SH HEMT	DH HEMT (high density)	DH HEMT (low density)
Si-planar I (AlGaAs)	$5X10^{12}cm^{-2}$	$5X10^{12}cm^{-2}$	$3X10^{12}cm^{-2}$
Si-planar II (GaAs)	–	$1X10^{12}cm^{-2}$	$1X10^{12}cm^{-2}$

In addition, we discuss the relation between the intrinsic HEMT device physics and their phase-noise performance, then propose a unique mechanism of the reduction in the phase noise at a high drain bias.

II. DEVICE FABRICATION AND CHARACTERISTICS

Fig. 1 shows a cross-sectional view of an AlGaAs/InGaAs pHEMT employed in the monolithic oscillators. There are three different kind of HEMT's fabricated: two DH HEMT's and a single-hetero (SH) HEMT. The DH HEMT's have double Si-planar doped layers in an AlGaAs and a GaAs layer. The double Si-planar doped layers in the GaAs layers have the same carrier density of 1×10^{12} cm^{-2}. However, the densities in the AlGaAs layers are different; one is 5×10^{12} cm^{-2}, the other is 3×10^{12} cm^{-2}. The SH HEMT has a Si-planar doped layer with a sheet carrier density of 5×10^{12} cm^{-2} in the AlGaAs layer. Table I summarizes the carrier densities. The gate length and width are 0.2 and 80 μm, respectively. The gate electrode is defined by a photo/electron beam (EB) hybrid exposure system with double-layer resist layers [14]. This process has excellent wafer throughput because it utilizes a step-and-repeat exposure procedure instead of EB lithography in fabricating the wide head of the T-shaped gate structure.

Fig. 2 shows the dependence of the drain current and the transconductance on gate voltage. The DH HEMT with the higher density has a higher maximum drain current ($I_{\max}$), while the lower doped DH HEMT has almost the same drain current capability as the SH HEMT. The pinchoff voltage of the DH HEMTs is about -1.4 V and that of the SH HEMT is about -0.8 V. The SH HEMT has the maximum transconductance among the three types of HEMT's, but sensitivity to the gate bias is large. In the case of the DH HEMT's, the sensitivity of the transconductance to the gate bias is fairly small and it is relatively high over the entire gate bias range. The maximum value for the SH HEMT is 650 mS/mm. The maximum transconductance of the DH HEMT with the higher density planar doped layer is 500 mS and that of the DH HEMT with the lower density planar doped layer is 425 mS/mm. The DH HEMT with the higher density planar doped layer exhibits a gate–drain break down voltage of 9 V under the condition of the gate leak current of 0.1 mA/mm. The lower density HEMT has a gate–drain breakdown voltage of 11 V and the SH HEMT exhibits a gate–drain breakdown voltage of 8 V.

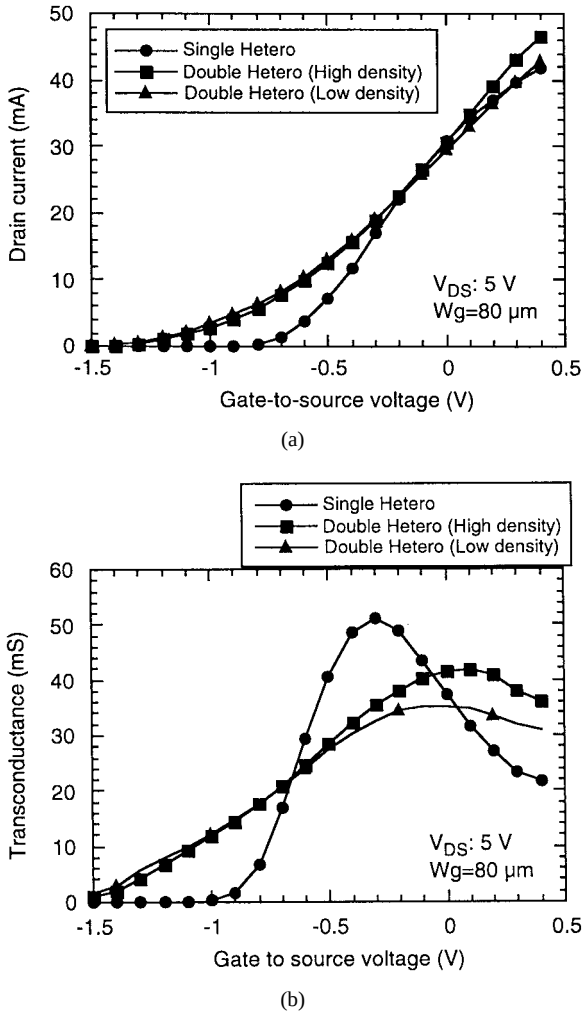


Fig. 2. (a) Dependence of the drain current on the gate-to-source voltage when biased at a drain voltage of 5 V. (b) Dependence of the transconductance on the gate-to-source voltage when biased at a drain voltage of 5 V.

III. DESIGN OF OSCILLATORS

Fig. 3 shows a circuit diagram of a V-band monolithic oscillator. The circuit configuration of the oscillator is a series feedback type with source inductors constructed by microstrip lines. $\Gamma_{\rm in}$ and Γ_d shown in Fig. 3 are defined as [15]

$$|\Gamma_{\rm in}| > \left|\frac{1}{\Gamma_d}\right| \tag{1}$$

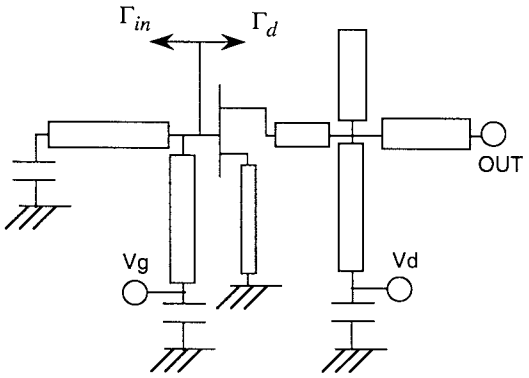


Fig. 3. Circuit diagram of the monolithic oscillator.

TABLE II
PARAMETERS OF A DH HEMT

Parameters		Parameters	
R_s [ohm]	1.5	γ	-0.18
R_d [ohm]	2.3	V_{bi} [V]	0.53
R_g [ohm]	3.2	V_{p0} [V]	-0.53
R_i [ohm]	2.65	C_{gs0} [pF]	0.095
α[-]	9.1	C_{gd0} [pF]	0.02
I_s [nA]	205	τ [pS]	0.57
I_{dss} [mA]	10.2		

$$\mathrm{Ang}(\Gamma_{\mathrm{in}}) = \mathrm{Ang}\left(\frac{1}{\Gamma_d}\right). \tag{2}$$

The resonance circuit consists of a microstrip line and a metal–insulator–metal (MIM) capacitor. A quarter-wavelength high-impedance line is used for a gate bias circuit. In addition, an *RC* circuit is incorporated as a filter in order to avoid undesirable low-frequency oscillator. The gatewidth of the HEMT is 80 μm. A small-signal circuit simulation is performed in order to examine the condition for oscillation. Cold modeling is applied to obtain the small-signal parameters of the HEMT [16], and the Materka–Kacprzak model is used as a large-signal model of the HEMT. Device parameters used in designing are shown in Table II.

Fig. 4 shows a microphotograph of a fabricated monolithic oscillator. The chip size if 1.3 mm $\times$ 1.4 mm and the substrate thickness is 100 μm. MIM capacitors adopt an SiN passivated layer of a thickness of 1500 Å. The passivated layer of the HEMT is as thin as 1000 Å to reduce the effect of parasitic elements.

IV. OSCILLATOR CHARACTERISTICS OF HEMT'S

Fig. 5 shows a measurement setup for measurement of fabricated oscillators. Phase-noise values are obtained by direct reading from the spectrum analyzer. Fig. 6 shows the dependence of the output power of each HEMT oscillator on the drain voltage. The range of the drain voltage is 3–5 V. The output power of the DH HEMT oscillator is superior to that of

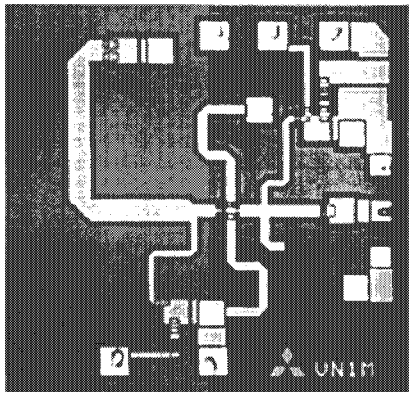


Fig. 4. Microphotograph of the fabricated monolithic oscillator.

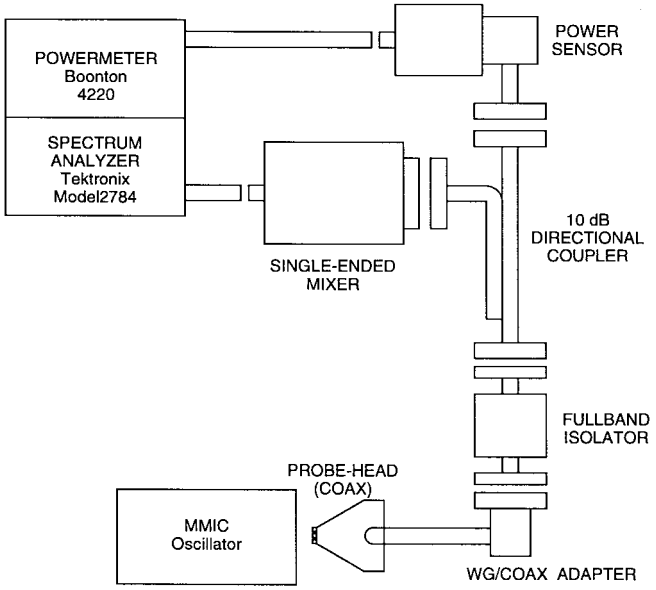


Fig. 5. Measurement setup for V-band oscillator.

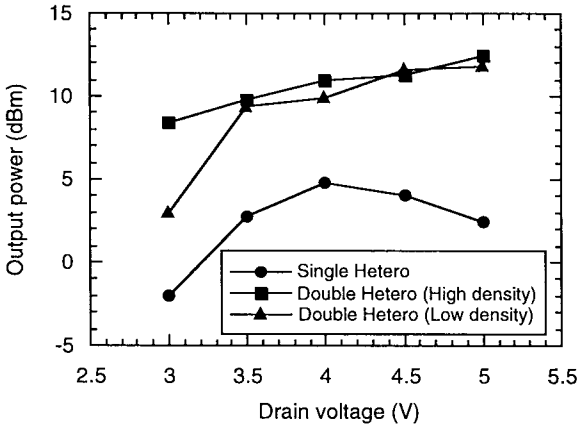


Fig. 6. Dependence of the measured output power performance on the drain voltage. The gate bias is 0 V.

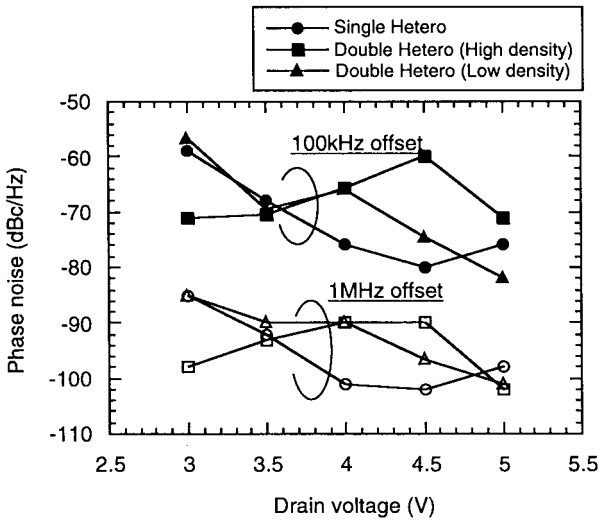


Fig. 7. Dependence of the measured phase-noise performance at 10-kHz offset and 1-MHz offset on drain voltage. The gate bias is 0 V.

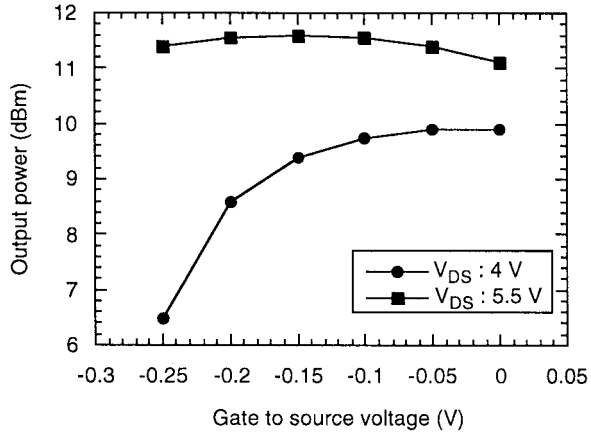


Fig. 8. Dependence of the output power on the gate voltage at drain voltages of 4 and 5.5 V.

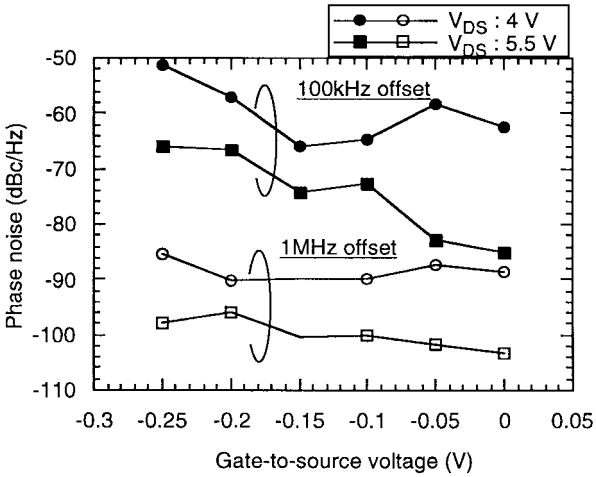


Fig. 9. Measured phase-noise performance at drain voltages of 4 and 5.5 V.

the SH HEMT: much more than 6 dB over the drain voltage from 3 to 5 V. The maximum output power of the DH HEMT oscillator with the higher density Si-planar doped layer is 12.4 dBm at a drain voltage of 5 V. The output power of the low-density DH HEMT oscillator is 0.5–1.0 dB lower than that of the higher density DH HEMT oscillator.

Fig. 7 shows the dependence of the measured phase noise performances at 100-kHz offset and 1-MHz offset on the drain voltage. For both offset frequencies, phase-noise shift versus drain voltage of the SH HEMT oscillator exhibits the similar curve of the output power. The phase-noise levels are achieved as -80 dBc/Hz at 100-kHz offset and -101 dBc/Hz at 1-MHz offset, both at a drain voltage of 4.5 V, which is the same bias point as the one when maximum output power is obtained. The phase noise of the SH HEMT oscillator decreases as the drain bias increases. However, the phase noise increases at drain voltage of more than 4.5 V, while the output power decreases. The phase noise of the high-density DH HEMT oscillator is -72 dBc/Hz at 100-kHz offset and -102 dBc/Hz at 1-MHz offset, both at a drain voltage of 5 V. In the high-density DH HEMT oscillator, the drain bias versus phase-noise performance is not conspicuous compared with the other types of HEMT materials. The phase noise of the lower doped DH HEMT oscillator is improved as the drain bias increases. The phase noise of -82 dBc/Hz at 100-kHz offset and -101 dBc/Hz at 1-MHz offset has been achieved when biased at a drain bias voltage of 5 V.

V. Oscillation Performance at High Drain Bias

The measured data indicated in Fig. 7 suggest that the oscillators exhibit better noise characteristics at higher drain voltage. We carried out a comparison of the characteristics (output power, phase noise, and pushing figure) of the oscillator with the lower doped DH HEMT oscillator. The dependence of the output power on the gate–source voltage is shown in Fig. 8 at a drain voltages of 4 and 5.5 V. Output power of more than 11 dBm has been obtained over the gate bias from 0 to -0.25 V at a drain voltage of 5.5 V. On the other hand, the output power at a drain voltage of 4 V is 1 dB lower than that of the one at the drain voltage of 5.5 V. Fig. 9 shows the phase noise performance at 100-kHz offset and 1-MHz offset. Phase noise is improved more than 10 dB at the higher drain voltage (5.5 V). The phase noise is also improved as the gate bias becomes positive. This corresponds with the phenomenon in which the pushing figure becomes small as the drain voltage increases. Fig. 10 shows the dependence of the oscillation frequency on the gate bias (pushing figure). The pushing figure becomes smaller at higher drain bias; 20 MHz/V at a gate bias of 0 V and a drain bias of 5.5 V. An oscillation spectrum is shown in Fig. 11 for the same bias voltage. A good spectrum is obtained. This output power provides the best performance among the oscillators without any buffer amplifiers around V-band [17]. In addition, the phase noise is comparable with that of HBT-based oscillators [18] and oscillators with dielectric resonators [5], [19], [20].

VI. Factors of Phase-Noise Reduction at High Drain Bias

There are several reports that the phase noise is minimized under a certain gate bias. The pushing figure is related to the phase noise, but the phase noise does not become minimum

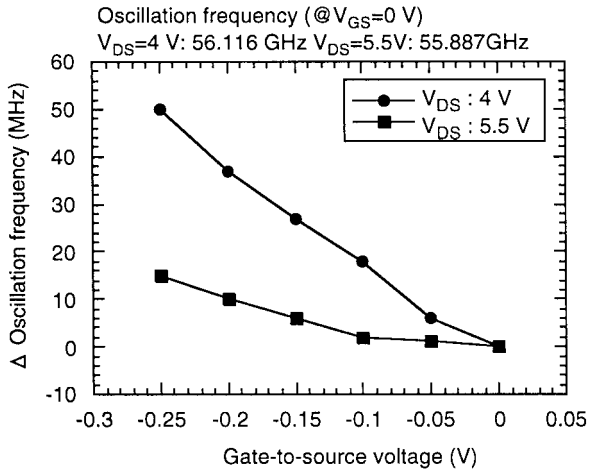


Fig. 10. Pushing figure of the oscillators and dependence on the gate voltage at drain voltages of 4 and 5.5 V.

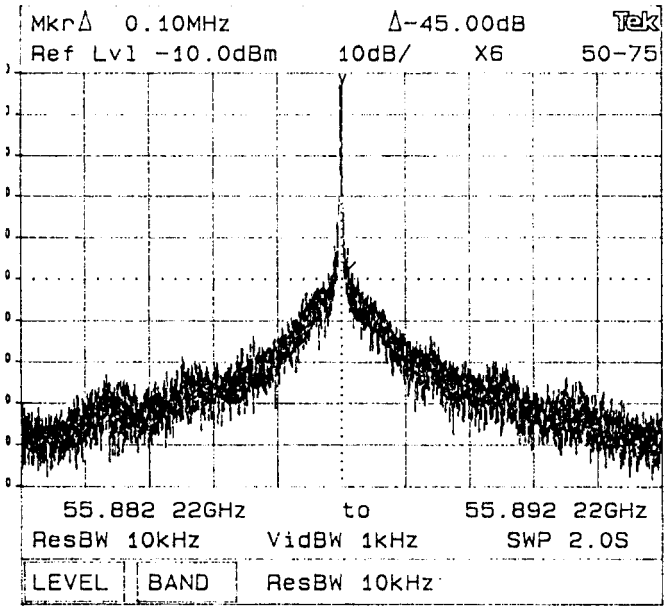


Fig. 11. Measured oscillation spectrum.

even if the pushing figure becomes minimum. Verdier *et al.* reported that they introduced the distributed effects of more than two noise sources and considered correlation between them to explain this phenomenon [7]. They report dependence on gate voltage, but there has been no report on the dependence on drain bias. In this section, the dependence of phase noise on the drain bias is investigated.

A. Gate–Source Capacitance

The depletion layer under the gate electrode is extended to the drain electrode, as shown in Fig. 12. The shape is changed by the drain voltage. The drain voltages that give the depletion layer A and B are defined as $VD(A)$ and $VD(B)$, respectively. The voltage of $VD(A)$ is smaller than that of $VD(B)$. The depletion layer near the source electrode is thinner when $VD(B)$ even at the same gate bias because the depletion layer is hauled toward the drain electrode. Fig. 13

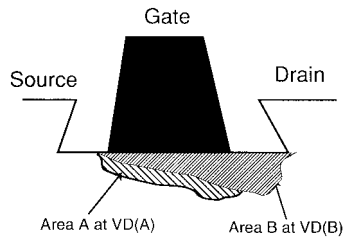
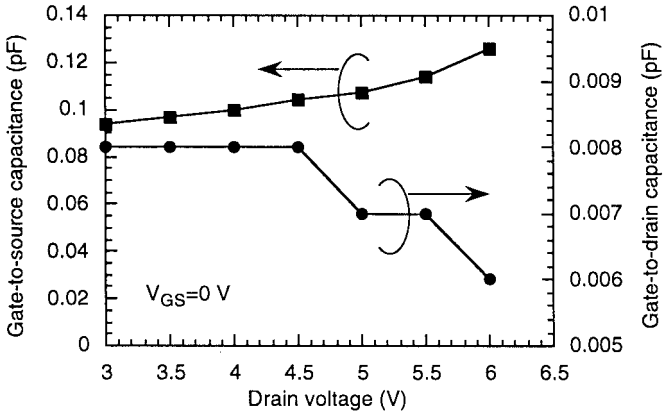
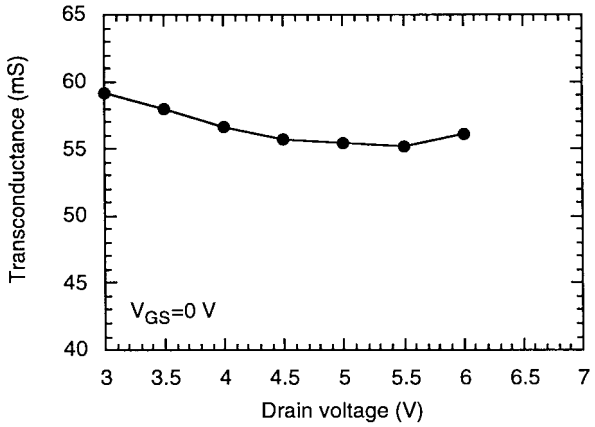


Fig. 12. Shape of the depletion layer under the gate electrode. Area A indicates the shape when biased at $VD(A)$. Area B indicates the shape when biased at $VD(B)$.



(a)



(b)

Fig. 13. Dependence of the extracted parameters on the drain voltage. (a) Gate capacitance. (b) Transconductance.

shows the gate-to-source capacitance and the gate-to-drain capacitance extracted from the measured S-parameters. During extraction, initial values of extrinsic parameters are calculated using S-parameters measured under the cold bias state and initial values of intrinsic parameters are extracted from the measured S-parameters under the hot bias state (operating bias point). Then, the initial values are fitted to the measured S-parameters. The calculated data show that the gate-to-source capacitance increases as the drain voltage increases. This increase of the gate-to-source capacitance means that the depletion layer is extended to the drain electrode. In Fig. 10, it is shown that pushing figure at a drain voltage of 5.5 V is much smaller than that at a drain voltage of 4 V. It can

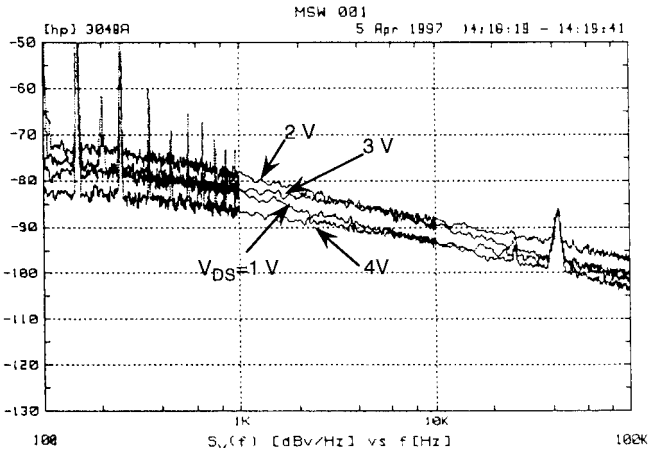


Fig. 14. Measured output low-frequency noise spectrum.

be considered that phase noise is improved by the change of the shape of the depletion layer depending on drain bias in conjunction with the dependence of oscillation frequency on the gate bias. Meanwhile, the change of the transconductance is small at drain voltage of more than 4 V. This fluctuation of the transconductance has less effect on the phase noise because the fluctuation mainly affects AM noise [12].

B. Dependence of $1/f$ Noise Spectrum on Drain Voltage

The spectrum of $1/f$ noise is one of the factors that determine the phase-noise characteristics of oscillators. Measurements of $1/f$ noise are widely used for investigations of phase-noise performances in HBT- and HEMT-based oscillators. In these investigations, the dependence of $1/f$ noise performance is studied with regard to the gate-to-source voltage of passivated films [21]. The measured $1/f$ noise spectrum, especially under the knee voltage, is also used for determination of device quality. There are several reports on investigations of the mechanisms about how $1/f$ noise is generated by measuring $1/f$ noise under a low drain bias, and many opinions about this mechanism [22], [23]. There are, however, few reports on the dependence of $1/f$ noise on drain voltage up to higher drain voltages where oscillators can operate.

Fig. 14 shows measured $1/f$ noise-voltage spectra at the drain terminal of the lower density DH HEMT. The gate voltage is 0 V. The $1/f$ noise voltage increases with a slope of -1 up to 2 V. The slope, however, becomes -0.8 at drain voltages in excess of 3 V. In addition, the noise voltage decreases as the drain voltage increases. A similar dependence is seen in measured phase noise versus drain voltage. There is no model that can describe this change of the slope. We discuss this change using the model of the $1/f$ noise in bulk. The $1/f$ noise that is generated from the bulk has the following characteristics as [24]: the $1/f$ noise is inversely proportional to a volume of a bulk, and the $1/f$ noise is inversely proportional to numbers of carriers in a bulk.

The former indicates a possibility that the channel is spread by the change of the shape of the depletion layer as the drain voltage increases. However, this spread of the channel should be caused under the relatively lower voltage. The weak impact ionization caused at a high drain voltage is one of the reasons that should be taken in consideration. A number of carriers can be generated by the weak impact ionization. In addition, it can be considered that the noise source created by the impact ionization may affect other noise sources.

VII. Conclusion

V-band high-power low-noise fundamental monolithic oscillators have been successfully developed. Comparison of oscillation performance is carried out among several HEMT structures, one SH structure and two DH ones. The output power of the DH HEMT oscillator is superior to that of the SH HEMT oscillator. The phase noise of the DH HEMT oscillator with lower density Si-planar layer is -85 dBc/Hz at 100-kHz offset and -103 dBc/Hz at 1-MHz offset with the high output power of 11.1 dBm at a drain voltage of 5.5 V. The measured phase noise is comparable with the one of the HBT-based monolithic oscillators.

The phase noise decreases as the gate-to-source voltage increases and decreases as the drain voltage increases. The depletion layer is extended to the drain electrode, then the sensitivity to the gate-to-source voltage becomes low at the higher drain voltage. This is one of reasons why the phase noise decreases as the drain voltage increases. The other reason is considered that weak impact ionization occurs at a certain drain voltage because the measured $1/f$ noise spectrum decreases and the slope of the spectrum changes at higher drain bias (more than 3 V). In addition, it may be considered that the noise source generated from the weak impact ionization has some correlation to the other noise sources.

Acknowledgment

The authors wish to thank Dr. Matsukawa for his encouragement. They gratefully appreciate M. Simozawa's support on $1/f$ noise measurement and also acknowledge the technical support from all the wafer-processing engineers.

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